2024 International VLSI Symposium on Technology, Systems and Applications

Call for Papers

April 22–25, 2024 Hsinchu, Taiwan

Paper Submission Deadline: 23:59 (GMT+8) Wednesday, December 06, 2023

Details:https://expo.itri.org.tw/2024VLSITSA

Highlights

The 2024 International VLSI Symposium on Technology, Systems and Applications will be held on April 22-25, 2024 at the Ambassador Hotel, Hsinchu, Taiwan.

The 4-day symposium will include:

- 3 Plenary Sessions
- 7 Special Sessions
- 2 Joint Special Sessions
- 3 Tutorials
- 2 Industrial Sessions
- The outstanding papers

Paper Submission

Prospective authors are invited to submit papers through the symposium website. All paper presenters are required to register for the symposium and accepted papers MUST be presented in person by one of the authors at the symposium, and the presentation must be conducted in English. All accepted manuscripts in the proceeding will be published in IEEE Xplore. No-show papers will not be included in the symposium proceedings and will not be submitted to the IEEE Xplore database.

TSA Scope: Submission to TSA https://expo.itri.org.tw/2024TSA/Submission

- Front-end CMOS and foundry technology
- Standalone memory: DRAM, FLASH, emerging memory technology
- Ultra-low power CMOS and embedded memory
- Advanced process modules: e.g. gate stack, junction, strain/channel engineering, low-R contact, low-C spacer/ILD, interconnect technology, ALE and selective deposition, etc.
- Nano-patterning: multiple patterning, directed self-assembly, EUV, etc.
- Advanced CMOS process and devices: Ge, SiGe, III-V, FinFET, GAAFET, low-dimensional materials and devices, 2D and nanowire devices
- BEOL compatible devices for 3D integration
- Material, process and device modeling
- Reliability physics, characterization and measurements
- Advanced packaging and 2.5D/3D integration
- TFT and organic electronics
- MEMS, imagers and sensors
- Power and analog IC devices and technology
- Photonics and beyond CMOS technology
- RF & THz process, device and integration technology
- Energy harvesting technology
- Wearable and IoE enabling technologies
- Quantum phenomena and information technologies
- Neuromorphic devices and materials for brain-inspired computing
- Device/circuit technologies for AI deep learning applications
- Advanced manufacturing technology, metrology and yield
- Emerging Materials and Devices

DAT Scope: Submission to DAT https://expo.itri.org.tw/2024DAT/Submission

■ Analog, Mixed-Signal, and RF Design

- Analog and Mixed-Signal Circuits
- Power Management Circuits
- Wireless Transmitter and Receiver Circuits
- Wired System and IO Design
- Sensor and Interface Circuits

■ Digital, Memory, and AI Chip Design

- Asynchronous and Neuromorphic Computing Circuits
- Communication Baseband Designs
- Computing-in-Memory
- Digital AI Chips
- Digital Circuits and ASICs
- Hardware Security and Trust
- Low Voltage & Ultra Low-Power Circuits and Systems
- Memory Circuits and Systems
- Security Circuits for IoT and AI
- Specialized Hardware

■ Emerging Technology

- Circuit & IP Design Based on New Transistor Technology, e.g., Fork-Fin FET, Sheet FET, GAA FET, and C-FET
- Cryogenic Circuits and Systems
- Flexible and Printable Electronics
- Medical/Bio-electronics/Bio-inspired Chip Designs
- Quantum Computing
- Silicon Photonics

■ Application, Software and Hardware, and AI System

- AI for Systems and Systems for AI
- CPU, DSP, and Multicore Architectures
- Domain-Specific Architectures and Accelerators
- Embedded System and Software
- Hardware-efficient AI Methods
- Multimedia Processing Designs
- SoC (System on Chip) and NoC (Network on Chip)
- Software/Hardware Co-Design and System Compiler
- SiP (System-in-Package) and Heterogeneous Integration

■ Design Automation and Test Methodology

- AI for Design Automation & Test
- Behavioral, Logic, and Physical Synthesis
- Design Automation & Test for Analog/Mixed-Signal/RF, 2D/3D IC, Memory, Biochip, AI Chips, and Emerging Systems
- Design for Manufacturability, Testability, and BIST
- Design Verification, Modeling, and Simulation
- Power/Thermal/Timing Optimization and On-Chip Monitoring
- Silicon Debug, Diagnosis, ECO, and Yield/Reliability Enhancement
- Test Generation, Compression, and Test Standards

General Chair

Shih-Chieh Chang
Industrial Technology Research Institute

TSA Symposium Chairs

Peide Ye
Purdue University

Jenn-Gwo Hwu
National Taiwan University

TSA Program Chairs

Tri-Rung Yew
National Tsing Hua University

Wei-Chung Lo
Industrial Technology Research Institute

DAT Symposium Chairs

Atsushi Takahashi
Tokyo Institute of Technology

Chih-Tsun Huang
National Tsing Hua University

DAT Program Chairs

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Intel

Chih-Wei Liu
National Yang Ming Chiao Tung University

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VLSI SINCE 1983

2024 International VLSI Symposium on Technology, Systems and Applications

ITRI Industrial Technology Research Institute

April 22–25, 2024 Hsinchu, Taiwan

TSA Call for Papers

The 2024 International VLSI Symposium on Technology Systems and Applications (VLSI TSA) will be held on April 22-25, 2024 at the Ambassador Hotel Hsinchu, Taiwan. Original and unpublished papers on all aspects of advanced VLSI technology and applications are solicited.

SCOPE

- Front-end CMOS and foundry technology
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PAPER SUBMISSION GUIDELINES

1. Camera-ready manuscript (**2 pages** including figures and tables) should be submitted electronically in PDF format through the symposium website at https://expo.itri.org.tw/2024TSA/Submission.
2. Accepted papers **MUST** be presented by one of the authors **in person** at the symposium to guarantee publication in the symposium proceedings. Presentations will be in English and will be limited to 15 minutes, with an additional 5 minutes for discussion.
3. Any changes on the title or author list or withdrawal after acceptance must be approved by Mentors or TSA Program Chairs.
4. All papers presented at the symposium will be published in the proceedings as submitted without revisions. Authors of accepted papers must transfer copyright to IEEE by utilizing the electronic IEEE Copyright Form (eCF) for inclusion in the IEEE Xplore database.
5. All paper presenters are required to register for the symposium.
6. No-show papers will not be included in the symposium proceedings, nor will they be submitted to the IEEE Xplore database.

STUDENT SUBSIDY

Student Travel Financial support for attending 2024 VLSI TSA is available for full-time student presenters living outside of Taiwan.

BEST STUDENT PAPER AWARD

The selection will be based on the paper quality evaluated by technical committee members, as well as the presentation of the paper at the symposium. The paper should be presented by the key author who is a full-time student at the time of paper presentation. The Best Student Paper Award will be presented to the winning student at the next year's symposium.

LATE NEWS PAPERS

A very limited number of high quality Late News Papers will be accepted. Note that Late News Papers are not eligible for the best student paper award.

IMPORTANT DATES (Note: All are based on Taiwan time, which is eight hours ahead of Greenwich Mean Time (GMT+8).)

Paper Submission Deadline	**Dec. 6, 2023**
Notification of Acceptance	Jan. 31, 2024
Late News Paper Submission Deadline	Feb. 15, 2024
Final Paper Submission	Feb. 28, 2024
Author Registration Deadline	Feb. 28, 2024

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■ Analog, Mixed-Signal, and RF Design

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- Power Management Circuits
- Wireless Transmitter and Receiver Circuits
- Wired System and IO Design
- Sensor and Interface Circuits

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- Power/Thermal/Timing Optimization and On-Chip Monitoring
- Silicon Debug, Diagnosis, ECO, and Yield/Reliability Enhancement
- Test Generation, Compression, and Test Standards

GENERAL INSTRUCTIONS

- Prospective authors must electronically submit the self-contained paper with figures and tables via the conference submission page (https://expo.itri.org.tw/2024DAT/Submission) before December 6, 2023 (23:59 GMT+8).
- The submitted manuscript must be 2 or 4 pages including references, double-columned, IEEE-style compatible, in PDF format only. Any submissions not adhering to the rules will be rejected immediately without review.
- Before submitting your abstract/paper, please review the information on IEEE Intellectual Property Rights at https://www.ieee.org/publications/rights/index.html
- The review process will be **double-blind**.
  - Please do NOT reveal any authors' information (names, affiliations, email, grant information, personal acknowledgment, etc.) anywhere in the initial manuscript. You must also ensure that the metadata in the PDF does not include such information.
  - All references, including authors' previous work, should be referred as 3rd-persons' works. E.g., you should use "This paper presents a new method to improve XXX's approach [1]." instead of "This paper presents a new method to improve our previous approach [1]." Do NOT omit or anonymize references for blind review.
  - The initial manuscript violating the double-blind review policy will be rejected.
- Accepted papers **MUST** be presented **in person** by one of the authors at the symposium, and the presentation must be conducted in English. All accepted manuscripts in the proceeding will be published in IEEE Xplore.
- Any changes on the title or author list or withdrawal after acceptance must be approved by DAT Program Chairs.
- All paper presenters are required to register for the symposium.
- No-show papers will not be included in the symposium proceedings and will not be submitted to the IEEE Xplore database.
- Please refer to the detailed information on the conference website for authors: https://expo.itri.org.tw/2024VLSITSA

STUDENT SUBSIDY

- Student Travel Financial support for attending 2024 VLSI TSA is available for full-time student presenters living outside of Taiwan.

BEST PAPER AWARD

Three best papers will be selected this year through a rigorous evaluation process conducted by the DAT technical program committee and session chairs.

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